An Integrated Recording System Using an Asynchrous Pulse Representation

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Abstract—**This paper describes a neuronal recording system based on asynchronous biphasic pulse coding. This system demonstrates the first step of developing a complete solution with fully integrated circuit architecture with applications to brain-machine interfaces. A parallel recording experiment comparing a commercial recording system (Tucker-Davis Technology (TDT)) and UF's custom recording system is set up to compare performance. The novel aspect of the UF system is that its output is represented by an asynchronous pulse train, which provides a low-power, low-bandwidth, noise-resistant means for coding and transmission. Taking advantage of neural firing features, the pulse-based approach uses 3K pulses/second to record from a hardware neural simulator.**

I. INTRODUCTION

A major goal of neuroscientists is to better understand the function of the brain and its complex distributed representations [1]. Neural signals, measured through action potentials, are a direct way to observe brain activity. Thus, extracting good quality extracellular neural action potentials is a top priority for brain-machine interfaces (BMIs) [2], which focuses on analysis of extracted information from neural recordings to create predictive models for animal or human movement.

There is a growing demand for wireless, low-power neural recording systems to amplify and transmit data, but current instrumentation technology has been a bottleneck to transfer large bandwidth data streams without being tethered with wires for hundreds of recording channels. For extracellular single neuron recording, each channel is typically sampled at 25 KHz (or greater) with 16-bit samples leading to a large 400 Kbits/second bandwidth for just one channel. Therefore, data compression is clearly a key challenge for future improvement of these implantable devices. The difficulty in data reduction arises from the requirement of small size and low power for implanted circuitry. Small size is due to the space limitations at the site of implantation and low power is necessary because of the difficulty of changing or charging implanted batteries. We propose a customized recording system scheme with bidirectional communication capability achieving miniaturization via CMOS integration of electronic components, power and bandwidth reduction via the novel pulse-based signal representation of neural signals.

The proposed recording system design for the parallel recording set-up is discussed in section II. Section III then describes the testing with the hardware neural signal simulator as the signal source, followed by a complete analysis of the recording data using spike sorting algorithms.

II. SYSTEM DESIGN

The neural recording platform was tested with Bionic's 128-channel hardware neural signal simulator as the signal source, which produces three different shaped action potentials on each of 128 channels. The simulation on each output channel consists of a sequence of three individual action potentials that fire one after the other at a 1-second interval. Then a one-second burst of activity is fired every 10 seconds, which consists of the same train of three individual action potentials with an interspike interval of 10 milliseconds.

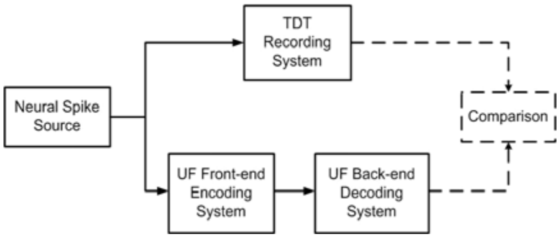

Figure 1. Parallel recording concept.

To verify the performance of the UF recording platform, we constructed a parallel recording as shown in Fig. 1. The UF recording system is divided into front-end and back-end parts. The major novelty of the UF recording system is to shift the signal processing load to the digital back-end which does not have strict constraints on power consumption, noise, and size. The task of the front-end part is to amplify the sensed signal and encode the information into a pulse-based format to transfer to the back-end part. The back-end decodes by reconstructing the original signal from the received pulses. This pulse coding idea facilitates the implementation of wireless implantable recording electrodes, which requires simple and small size front-end analog circuit design attached on the implanted electrodes to transmit information wirelessly with limited bandwidth for low power consumption to back-end for post signal processing.

A. TDT Recording System

A bench-top laboratory recording system is used evaluate the performance of the UF implantable recording platform. Tucker-Davis Technology (TDT, Alachua, Florida) is a well-known company providing integrated hardware and software solutions for data acquisition and analysis. The PZ-2 64 channel preamplifier and System 3 real-time signal processing system are installed in the computer, which digitizes amplified analog signals at ~12.2kHz. A digital band pass filter (300 ~ 5k Hz) used to isolate single neuron activity was implemented in software and was designed to have the same bandwidth as UF recording system for display on the screen.

B. UF Recording System

1) Bioamplifer: The structure of the bioamplifier was originally proposed by Harrison [3] . The midband gain Am is designed to be 40 dB, the lower corner frequency is ~0.3Hz and the higher corner frequency is 5k Hz. An external lumped circuit high pass filter (300 Hz) follows the output of the bioamplifer to remove major electromagnetic contamination of 60 Hz and its harmonics.

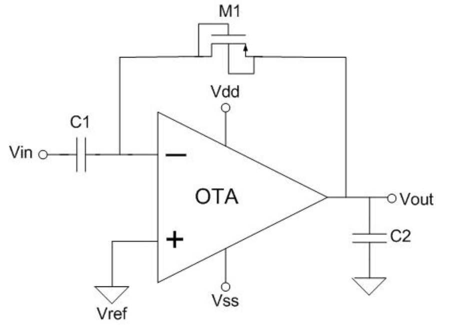

Figure 2. Schematic of current generator and integrator

2) Current Integrator: Figure 2 shows the schematic of the current generator and the integrator, where M1 is a single diode-connected PMOS transistor. It acts as a “pseudo-resistor” with a resistance greater than $10^{11}\Omega$ [4]. The operating point of the operational transconductance amplfier (OTA) is defined by Vref. The OTA converts the AC voltage signals of interest into a current while blocking DC offsets using coupling capacitor C1. Capacitor C2 works as an integrator. Utilizing a single transistor to act as the pseudo resistor has the advantage of reduced leakage currrent than two diode-connected transistor design [5], which leads to Vout bias voltage deviation and asymmetric biphasic ouptut of IF circuit.

3) Integrated-and-Fire Circuit: The biphasic encoding mechanism can be realized using electronic circuits [5]. The cuurent integrator feeds its integrated voltage on a capacitor to inputs of two comparators. A positive and a negative threshold voltage are set for each comparator to generate biphasic outputs depending on the input signal polarity. Each comparator is followed by an asymmetric delay circuit which postponds the falling edge of pulses. This design is employed to generate a refractory period. This biphasic IF circuit can encode postive and negative signals without additional DC voltage shifts for monophasic operation, which generates pulses without signals but DC at the input.

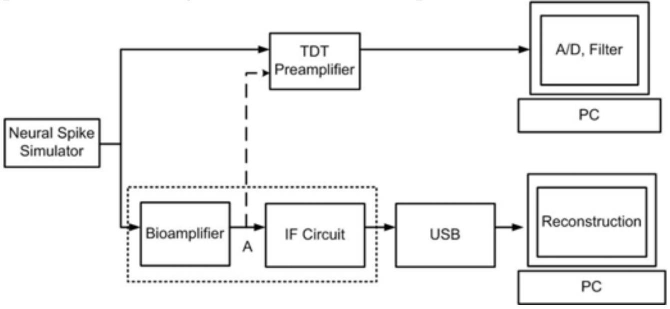

Figure 3. Configuration of parallel reocording system block diagram. The dashed box is illustrated as a photo in Figure 4.

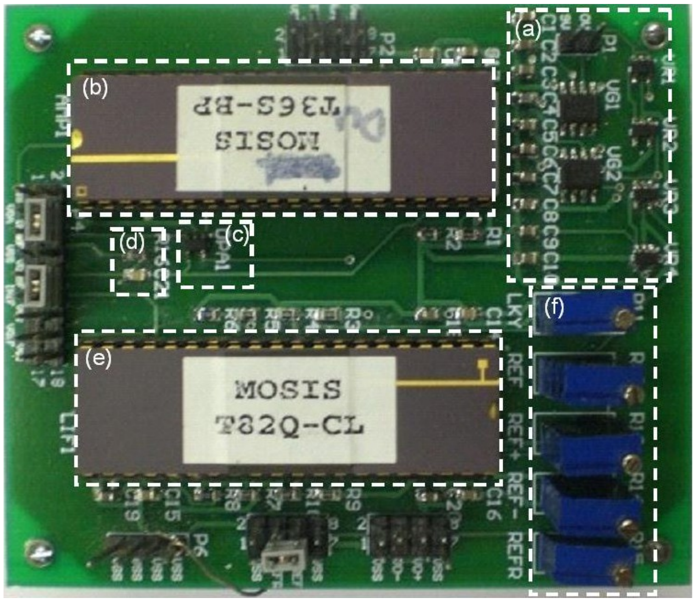

Figure 4. PCB photo: integration of bioamplifier and the IF circuit: (a) Power regulator circuitry for the whole PCB, (b) Bioamplifier chip to amplify and filter neural signals, (c) Buffer at output of the amplifier, (d) High pass filter to attenuate 60Hz noise, (e) Integrate-and-fire (IF) chip to code information into pulses, (f) Variable resistors to adjust IF parameters.

4) USB Recording Board: The biphasic pulses are recorded using the SimpleMonitorUSBxpress board developed by Dr. Tobi Delbrück, at the Institute for Neuroinformatics (INI) in Zurich, Switzerland. Whenever a pulse is generated by the biphasic neuron, the request pin on the USB board is pulled low generating an interrupt signal. The board time stamps the pulse and records the timestamp and address that were generated the interrupt in its internal RAM. The microcontroller then pulls the acknowledge signal low and the request signal is pulled high, indicating that the handshake is completed. For our biphasic neuron, the reset signal for the neuron is connected to the request signal on the USB board. Once the interal RAM is full, the address and timestamps are sent to the host, a computer in this case. These timestamps are captured on the microcontroller using an internal 1µs clock and a 16-bit timer, allowing for 65ms of events on the device. Timestamps are unwarped on the host to a 32 bit resolution providing a maximum timestamp of about 4300 seconds.

5) Reconstruction Algorithm: It is well established that the family of sinc functions is a frame for the band limited space therefore any band limited function can be expressed as a countable linear combination of these elements. Assume x(t) is band limited then:

$$x(t)=\sum_j c_j \sin c_\Omega (t-m_j) \tag{1}$$

where c_j is a weighted coefficient for each sinc function, Ω denotes the bandwidth of the signals and

$$m_j=\frac{t_{i+1}+t_i}{2} \tag{2}$$

The signals from the IF sampler can actually be rewritten in terms of the frame.

$$\theta_i=\int_{t_i}^{t_{i+1}} x(t)g(t)dt=\sum_j c_j \int_{t_i}^{t_{i+1}} \sin c_\Omega (t-m_j)g(t)dt \tag{3}$$

In matrix notation we rewrite (3) to $\Theta = SC$. Therefore in order to obtain the coefficient vector 'C' for the reconstruction we should invert the S matrix, this matrix is usually ill conditioned and iterative methods are used to obtain a stable solution. In this case we use a simpler algorithm for fast reconstruction that only takes into consideration local information from the samples. This simple algorithm estimates the reconstructed values of the signal right on the sample times and, a nearest neighbor interpolation is used to estimate the values on the uniform grid points. This produces a staircase like signal which is finally low pass filtered.

III. HARDWARE TESTING AND ANALYSIS

Figure 3 illustrates the parallel recording system block diagram for the experiment. The same signal source is fed into both recording paths at the same time. The output signals recorded from both systems are aligned and compared. For the bottom path, the UF recording system consists of a bio amplifier, an integrate-and-fire (IF) circuit, and a USB interface board connected to a computer with the reconstruction algorithm for the back-end process. The bio-amplifier and IF circuit are custom CMOS integrated chips mounted on the same print circuit board, as revealed in Fig. 4. The IF circuit chip includes the current integrator circuit to provide positive and negative signals to the IF circuit.

In order to verify the functionality of the IF circuit in the front-end part and the reconstruction algorithm in the back-end part, an additional signal connection from point A (Fig. 3) to the TDT preamplifier is made to collect and save to disk a digitized form of the input to the IF chip. As a result, output signals of the bio-amplifier and reconstructed signals can be compared and analyzed in this experiment. Positive and negative threshold are set ±250mV individually. The refractory period is adjusted to 10 µs and pulse rate is on average ~2k pulses/sec, providing a tremendous compression of the neural signal.

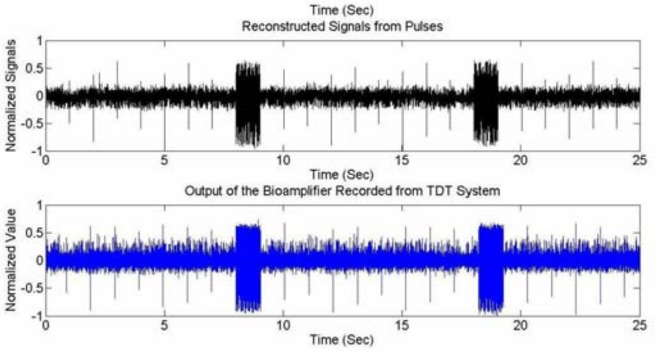

Figure 5. Comparison between reconstructed signals (top) and neural spike simulator signal (bottom) recorded through TDT system.

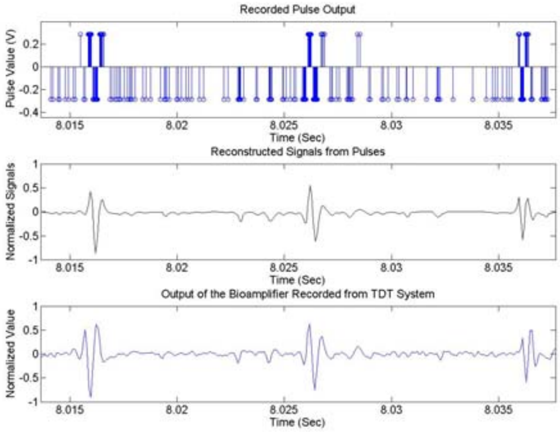

Figure 6. Alignment of three signals: recorded pusles through USB (top), reconstruction siganl at the back-end of UF recording system (medium), and ouput signal of bioamplifiers recorded through TDT recording system.

A. Neural Signal Simulator Testing

Figure 5 shows the comparison between voltage time series of the recording output signal of the bio-amplifier and the reconstructed signals. This is a 25-sec long recording with normalized values. The bottom plot shows the current signals reconstructed from pulses. The current integrator circuit is assumed to transfer voltage signals at the output of the bio-amplifier to current. Action potentials are clearly observed on both channels.

B. Reconstruciton and Comparison

Figure 6 displays the comparison among the recorded pulses, the reconstructed signals from pulses and TDT recorded signals at a zoom-in scale of ~25ms. Three distinct neurons are seen in order with an interspike interval of 10ms. Reconstructed spike times correspond to more dense recorded pulses. The IF representation does introduce some distortions in the relative ratio of the depolarization, repolarization, and hyperpolarization phases of the action potential. This observation is affected by the parameters used to encode the waveform and represents a tradeoff between bandwidth and accuracy of reconstruction (perfect reconstruction can be achieved at the cost of higher bandwidth). In this experiment, lower bandwidth was chosen and it was observed that the distortions are unique and consistent with each neuron type. This observation opens the possibility of spike sorting as is performed in multi-electrode array experiments.

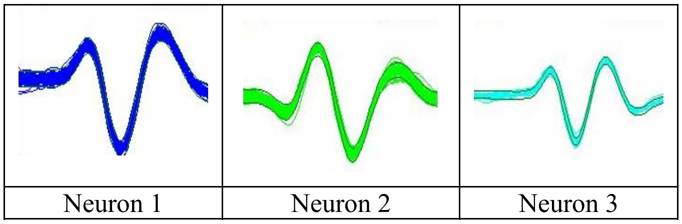

Figure 7. Neural spike waveform plie plot from outputs of bio-amplifiers

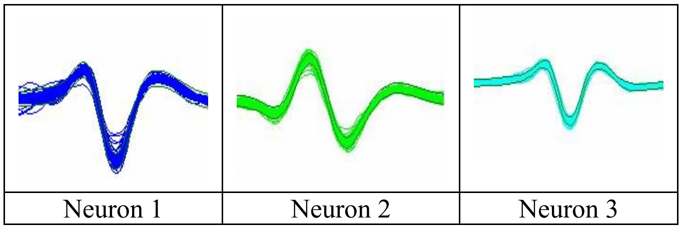

Figure 8. Neural spike waveform pile plot from reconstrcted signals

C. Spike Sorting and Cross Correlation

To simulate how the recordings would be used in electrophysiological experiments, spike sorting implemented on the IF representation isolates action potentials from single neurons. Spike sorting is a classical method used by neuroscientists with many proposed algorithms in the literature [6]. Spike2 (CED, UK), a popular commercial program, which can spike sort offline, is used to analyze the recorded bio-amplifier outputs and the recorded signals. The spike sorting is performed with a combination of template matching and a principal component analysis (PCA) based cluster cutting [6]. Briefly, a threshold is first applied to the data to detect candidate waveforms. Figure 7 and 8 show the pile plots of each neuron waveform. Although three neurons can be distinguished in each recording individually, there is still some distortion observed for almost all peak portions of action potentials (see Fig. 8, Neuron 1) which affects the cross correlation coefficient shown in Table II. The reasons causing this may be from the imperfection of the parameters of the IF and reconstruction algorithms applied, and are subject of future experimentation and improvement. Timestamps of each classified neuron from both data sources are recorded and compared between these two spike sorting results. The results are listed in Table I and II. Three kinds of neurons are correctly confirmed with high matching rate low missed spike ratio, misdetection ratio, and misclassification ratio.

IV. CONCLUSIONS AND FUTURE WORK

An implementation of an asynchronous biphasic pulse-based neural recording system is presented. This system is examined in parallel recording with a commercial recording system. Spiking sorting results verify that the performance of the UF customized recording system is compatible with conventional products and high performance spike sorting is possible. Three neurons are still distinctly classified and separated through PCA procedure. Although reconstructed action potentials are distorted, they are consistent and ongoing efforts are directed to improve the reconstruction. These include optimization of the IF parameters and better reconstruction algorithms. High matching rate between spikes of the output of amplifiers and that of reconstructed signals demonstrates the feasibility of asynchronous biphasic pulse neural signal recording. Low-power and noise-resistant IF neuron circuit operating as a hardware spiking neuron transmits only 2K pulses/sec and can act as the ADC in BMI applications. Recall from earlier that one channel can take as much as 400K bits/sec. An advantage of this demonstration is to make a step forward to fully integrated circuit and battery-powered system for wireless transmission with much less average bandwidth of neural recording for brain-machine interfaces. Rat neural recording is ongoing and will be presented in the full paper.

TABLE I.
SPIKE SORTING RESULT OF RECONSTRUCTED SIGNALS

Missed spike ratio	**Misdetection ratio**	**Misclassification ratio**
0.45%	0.45%	0.45%

TABLE II.
PERFORMANCE OF RECONSTRUCTION AFTER RECORDING

	Neuron 1	**Neuron 2**	**Neuron 3**
Matching Rate	98.67%	100%	98.63%
Cross Correlation Coefficient	0.84	0.83	0.69

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